that the selection ratio of the GaAs or InGaAs layer to the AlGaAs layer is high. This technique appears to produce similar effects by substituting the AlGaAs layer for the InGaP layer. However, this is difficult for the reasons described below.

[0169] First, the dry etching technique unavoidably causes defects in a substrate which may degrade the characteristics of the transistor.

[0170] Second, AlGaAs has a lower electron affinity than InGaP. AlGaAs thus creates a large energy discontinuous area in a conduction band in an AlGaAs/GaAs interface or an AlGaAs/InGaAs interface. Accordingly, when electrons flow from the GaAs or InGaAs layer to the AlGaAs layer, they must pass over an energy barrier of, for example, about 300 mV. This may increase a contact resistance.

[0171] In contrast, according to the manufacturing method of each embodiment of the present invention, the recess etching comprises wet etching. This prevents defects in the substrate which may degrade the characteristics of the transistor. Furthermore, InGaP has a relatively high electron affinity. InGaP thus creates only a small energy discontinuous area in a conduction band in an InGaP/GaAs interface or an InGaP/InGaAs interface. Accordingly, when electrons flow from the GaAs or InGaAs layer to the GaAsP layer, they have only to pass over an energy barrier of, for example, about 30 mV or less. This suppresses an increase in contact resistance.

[0172] In the above embodiments, the lower electron supply layer **13** and upper electron supply layer **15**, each composed of n-AlGaAs, need not contain a uniform amount of n type impurities. These layers may locally contain a higher concentration of type impurities. That is, the lower electron supply layer **13** and the upper electron supply layer **15** may be formed of AlGaAs partly or entirely doped with n type impurities.

[0173] Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

What is claimed is:

1. A heterojunction type compound semiconductor field effect transistor comprising:

a channel layer provided on a compound semiconductor substrate and composed of intrinsic GaAs or InGaAs;

a first electron supply layer provided on the channel layer and composed of AlGaAs doped with n type impurities;

an electric field strength reducing layer provided on the first electron supply layer and composed of intrinsic InGaP;

a first contact layer provided on the electric field strength reducing layer and composed of GaAs or InGaAs doped with n type impurities;

a recess stopper layer provided on the first contact layer and composed of intrinsic InGaP;

a second contact layer provided on the recess stopper layer and composed of GaAs doped with n type impurities of a concentration higher than that of the first contact layer;

a wide recess opening formed to penetrate the second contact layer so as to expose a surface of the recess stopper layer;

a narrow recess opening formed in the wide recess opening to penetrate the recess stopper layer, the first contact layer, and the electric field strength reducing layer so as to expose a surface of the first electron supply layer;

a gate electrode provided on the surface of the first electron supply layer exposed from a bottom of the narrow recess opening; and

a source electrode and a drain electrode provided on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode.

2. The heterojunction type compound semiconductor field effect transistor according to claim 1, wherein each of the electric field strength reducing layer and the recess stopper layer is thinner than the first contact layer.

3. The heterojunction type compound semiconductor field effect transistor according to claim 1, wherein the compound semiconductor substrate includes a semi-insulating GaAs substrate, a buffer layer provided on the semi-insulating GaAs substrate and having a superlattice structure, and a second electron supply layer provided on the buffer layer and under the channel layer and composed of AlGaAs doped with n type impurities.

4. A heterojunction type compound semiconductor field effect transistor comprising:

a channel layer provided on a compound semiconductor substrate and composed of intrinsic GaAs or InGaAs;

a first electron supply layer provided on the channel layer and composed of AlGaAs doped with n type impurities;

an electric field strength reducing layer provided on the first electron supply layer and composed of intrinsic InGaP;

a first contact layer provided on the electric field strength reducing layer and composed of GaAs or InGaAs doped with n type impurities;

a recess stopper layer provided on the first contact layer and composed of intrinsic InGaP;

a second contact layer provided on the recess stopper layer and composed of GaAs doped with n type impurities of a concentration higher than that of the first contact layer;

a wide recess opening formed to penetrate the second contact layer and the recess stopper layer so as to expose a surface of the first contact layer;

a narrow recess opening formed in the wide recess opening to penetrate the first contact layer and the electric field strength reducing layer so as to expose a surface of the first electron supply layer;